I claim

1. In an analog-to-digital converter having successive converter stages, a method of converting data signals and calibrating at least one converter stage, the method comprising the steps of:

with first sets of switched capacitors, processing data signals through said converter stages to provide corresponding data digital codes;

with a second set of switched capacitors in a selected one of said converter stages, generating an initial calibration signal interleavably with said data signals; and

with second sets of switched capacitors in downstream converter stages that are downstream from said selected converter stage and in response to said initial calibration signal, processing downstream calibration signals interleavably with said data signals to provide corresponding calibration digital codes.

2. The method of claim 1, further including the step of obtaining, from said calibration digital codes, calibration coefficients for said selected converter stage that correspond to its second set of switched capacitors.

3. The method of claim 2, wherein said obtaining step includes the steps of comparing said calibration digital codes to expected digital codes to thereby generate said calibration coefficients.

4. The method of claim 2, further including the step of storing said calibration coefficients.

5. The method of claim 2, further including the step of subsequently exchanging said first and second sets of switched capacitors in said selected converter stage.

6. The method of claim 5, further including the step of executing

said exchanging step on a random basis.

7. The method of claim 2, further including the step of successively repeating said generating and said downstream calibration signals processing step for converter stages that preceed said selected converter stage.

8. The method of claim 6, further including the step of continuously executing said generating and said downstream calibration signals processing step for said selected converter stage and for converter stages that preceed said selected converter stage.

9. In an analog-to-digital converter having successive converter stages, a method of interleavably converting data signals to corresponding data digital codes and calibrating at least one converter stage, the method comprising the steps of:

in each of said converter stages,

a) converting an input data signal to a corresponding data digital code in a first operational phase of that converter stage; and

b) arranging a first set of switched capacitors to receive said input data signal in said first operational phase and to provide, in a succeeding second operational phase of that converter stage, a succeeding input data signal for a succeeding converter stage, whereby the first and second operational phases of any one of said converter stages are respectively coincident with the second and first operational phases of an adjacent one of said converter stages;

in a selected one of said converter stages, arranging a second set of switched capacitors to receive an input calibration signal in said second operational phase and to provide a succeeding input calibration signal for a succeeding converter stage in said first operational phase; and

in at least one of downstream converter stages that succeed said selected converter stage,

a) converting an input calibration signal to a corresponding calibration digital code in said second operational phase; and

b) arranging a second set of switched capacitors to receive said input calibration signal in said second operational phase and to provide an input calibration signal for a succeeding converter stage in said first operational phase; and

from calibration digital codes of said downstream converter stages, obtaining calibration coefficients for said selected converter stage that correspond to its second set of switched capacitors.

10. The method of claim 9, further including the steps in said selected converter stage of:

exchanging said first and second sets subsequent to said obtaining step; and

providing the input data signal of the succeeding converter stage with said second set.

11. The method of claim 9, wherein said obtaining step includes the steps of comparing the calibration digital codes of said downstream converter stages to expected digital codes to thereby generate said calibration coefficients.

12. The method of claim 9, wherein:

said second-set arranging step of said selected converter stage includes the step of successively applying different decision signals to at least one capacitor of said second set in said first operational phase to thereby generate a difference in the calibration digital codes of said downstream converter stages; and

said obtaining step includes the step of comparing said difference

to a predetermined difference.

13. The method of claim 9, further including the step of narrowly spacing said input calibration signal of said selected converter stage from an input threshold of said selected converter stage in said second operational phase.

14. The method of claim 9, wherein:

said second-set arranging step of said selected converter stage includes the step of applying opposite-polarity input calibration signals to different capacitors of said second set in said second operational phase; and

said obtaining step includes the step of setting said calibration coefficients equal to the calibration digital codes of said downstream converter stages.

15. The method of claim 14, further including the step of applying a null decision signal to at least one capacitor of the second set of said selected converter stage in said first operational phase.

16. The method of claim 9, wherein:

said second-set arranging step of said selected converter stage includes the steps of:

a) applying a null decision signal to at least one capacitor of said second set in said first operational phase; and

b) successively applying opposite-polarity input calibration signals to the capacitors of said second set in said second operational phase to thereby provide a difference in the calibration digital codes of said downstream converter stages; and

said obtaining step includes the step of comparing said difference to a predetermined difference.

17. The method of claim 9, wherein:

said first-set arranging step includes the step of applying, to at least one capacitor of said first set, a data decision signal that corresponds to said data digital code; and

said second-set arranging step of said downstream converter stages includes the step of applying, to at least one capacitor of said second set, a calibration decision signal that corresponds to said calibration digital code.

18. The method of claim 9, wherein:

said first-set arranging step includes the step of switching at least one capacitor of said first set about an amplifier to facilitate provision of said input data signal for said succeeding converter stage; and

said second-set arranging step of said selected converter stage and said downstream converter stages includes the step of switching at least one capacitor of said second set about said amplifier to facilitate provision of said input calibration signal for said succeeding converter stage.

19. An analog-to-digital converter system that interleavably converts data signals to corresponding data digital codes and calibrates at least one converter stage, the system comprising:

a plurality of converter stages which each include:

a) an analog-to-digital converter that, in response to an input data signal, provides a corresponding data digital code in a first operational phase of that converter stage;

b) a first set of switched capacitors arranged to receive said input data signal in said first operational phase and to provide an input data signal for a succeeding converter stage in a succeeding second operational phase of that converter stage;

in a selected one of said converter stages, a second set of switched capacitors arranged to receive an input calibration signal in said second operational phase and to provide an input

calibration signal for a succeeding converter stage in said first operational phase; and

in at least one of downstream converter stages that succeed said selected converter stage, a second set of switched capacitors arranged to receive said input calibration signal in said second operational phase and to provide an input calibration signal for a succeeding converter stage in said first operational phase wherein the analog-to-digital converter of each of said downstream converter stages converts an input calibration signal to a corresponding calibration digital code in said second operational phase; and

a processor configured to obtain, from calibration digital codes of said downstream converter stages, calibration coefficients for said selected converter stage that correspond to its second set of switched capacitors.

20. The system of claim 19, further including a clock generator that provides clock signals to said first and second sets and wherein said processor is configured to:

command changes in said clock signals that exchange said first and second sets; and

alter said data digital code in accordance with said calibration coeffiecients.

21. The system of claim 19, wherein:

said selected converter stage includes a digital-to-analog converter that generates decision signals;

and said controller:

a) commands said digital-to-analog converter to apply different decision signals to at least one capacitor of said second set in said first operational phase to thereby generate a difference in the calibration digital codes of said downstream converter stages;

and

b) compares said difference to a predetermined

difference.

22. The system of claim 21, wherein said controller narrowly spaces said input calibration signal of said selected converter stage from an input threshold of said selected converter stage in said second operational phase.

23. The system of claim 19, wherein said controller:

applies opposite-polarity input calibration signals to different capacitors of the second set of said selected converter stage in said second operational phase; and

sets said calibration coefficients equal to the calibration digital codes of said downstream converter stages.

24. The system of claim 23, wherein said controller applies a null decision signal to at least one capacitor of least one capacitor of the second set of said selected converter stage in said first operational phase.

25. The system of claim 19, wherein said controller:

applies a null decision signal to at least one capacitor of the second set of said selected converter stage in said first operational phase;

successively applies opposite-polarity input calibration signals to the capacitors of the second set of said selected converter stage in said second operational phase to thereby provide a difference in the calibration digital codes of said downstream converter stages; and

compares said difference to a predetermined difference.

26. The system of claim 19, wherein each of said converter stages includes a digital-to-analog converter that:

in said second operational phase, applies a data decision signal to at least one capacitor of said first set that corresponds to said data digital code; and

in said first operational phase, applies to at least one capacitor of said second set of said downstream converter stages a calibration decision signal that corresponds to said calibration digital code.

27. The system of claim 19, wherein:
each of said converter stages includes an amplifier; and
said controller:

a) switches at least one capacitor of said first set about said amplifier to facilitate provision of said input data signal for said succeeding converter stage; and

b) switches at least one capacitor of said second set about said amplifier to facilitate provision of said input calibration signal for said succeeding converter stage.

28. The system of claim 19, wherein each of said converter stages includes a switch network that responds to said controller to thereby arrange said first and second sets of capacitors in said first and second operational phases.